



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/566,667

01/30/2006

Yushi Sekiguchi

AI 399NP

6051

23995

7590

11/26/2008

RABIN & Berdo, PC

1101 14TH STREET, NW

SUITE 500

WASHINGTON, DC 20005

EXAMINER

CHIU, TSZ K

ART UNIT

PAPER NUMBER

2822

MAIL DATE

DELIVERY MODE

11/26/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/566,667	<b>Applicant(s)</b> SEKIGUCHI, YUSHI	
	<b>Examiner</b> Tsz K. Chiu	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) 5-8 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/04/08, 12/15/06, 1/30/06</u> .                             | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

This Office Action is response to election/restriction filed 7/23/08.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (4654685).

With respect to claim 1 and 3, Yamada discloses for example in figure 2, 6, 13, and 14

a photoelectric conversion device (10); and

a drive circuit (figure 12) that drives the photoelectric conversion device

a photoelectric conversion layer (14B,14G,14R) of a first conductivity type, the photoelectric conversion layer being stacked on a semiconductor substrate (11R); and

an element dividing region (16B,16R,16G) of a second conductivity type, the element dividing region being formed in the photoelectric conversion layer, the element dividing region dividing the photoelectric conversion layer into a first photoelectric conversion region (14B), a second photoelectric conversion region (14G), and a third photoelectric conversion region (14R) along the semiconductor substrate;

a first dividing region (16B) of the second conductivity type, the first dividing region being formed at a predetermined depth from a surface of the photoelectric

Art Unit: 2822

conversion layer in the first photoelectric conversion region, the first dividing region dividing the first photoelectric conversion region into a first surface side region closer to the surface thereof and a first substrate side region closer to the semiconductor substrate, the first dividing region having a through hole (figure 4) through which the first surface side region and the first substrate side region communicate with each other;

a second dividing region (16G) of the second conductivity type, the second dividing region being formed at substantially the same depth as the first dividing region or at a shallower depth than the first dividing region in the second photoelectric conversion region (14G), the second dividing region dividing the second photoelectric conversion region into a second surface side region closer to the surface thereof and a second substrate side region closer to the semiconductor substrate; and

a third dividing region (16R) of the second conductivity type, the third dividing region being formed at a shallower depth than the second dividing region in the third photoelectric conversion region, the third dividing region dividing the third photoelectric conversion region (14R) into a third surface side region closer to the surface thereof and a third substrate side region closer to the semiconductor substrate.

With respect to claim 2 and 4, Yamada discloses for example in figure 2, 6, 13, and 14

a photoelectric conversion device (10); and

a drive circuit (figure 12) that drives the photoelectric conversion device

a photoelectric conversion layer (14B,14G,14R) of a first conductivity type, the photoelectric conversion layer being stacked on a semiconductor substrate (11R); and

Art Unit: 2822

a dividing region (16B,16G,16R) of a second conductivity type, the dividing region being formed at a predetermined depth from a surface of the photoelectric conversion layer, the dividing region dividing the photoelectric conversion layer into a surface side region closer to the surface thereof and a substrate side region closer to the semiconductor substrate, the dividing region having a through hole (figure 4) through which the surface side region and the substrate side region communicate with each other.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 571-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 10/566,667  
Art Unit: 2822

Page 5

/Zandra V. Smith/  
Supervisory Patent Examiner, Art  
Unit 2822

TC